REMARKS

Applicants appreciate the thorough examination of the present application as evidenced by the Office Action. However, Applicants request withdrawal of the rejections for at least the reasons discussed below.

The Section 102 Rejections:

Claims 1-24 stand rejected under 35 U.S.C. § 102(b) as anticipated by United States Patent No. 5,774,476 to Pressly *et al.* ("Pressly"). Office Action, p. 3. In particular, with respect to independent Claims 1, 4, 13-16, 20 and 21, the Office Action asserts, among other things, that the embedded core 14 and customer specified logic 12 of Pressly correspond to the core and input side sub logic circuit of Claim 1 and the mux 42 in Figure 2 of Pressly discloses the multiplexer between the core block and input side sub logic circuit unit. Office Action, pp. 3-4. Claim 1 has been amended above to recite that the MUX unit is between the core block and the input side sub logic circuit "without synchronizing" between the core block and the MUC unit. Similar amendments have made to each of the other independent claims.

As discussed in the present specification, various prior art approaches require that each port of the core block be included in a peripheral scan test circuit. Specification, p. 2, line 16 to p. 3, line 4. Examples of such peripheral scan test circuitry, shown in Figures 2-4, include multiplexers as well as flip-flops to provide synchronization to a system clock. In contrast, as described in the present specification:

> According some embodiments of the present invention, when scan test circuits, whose number is the same as the number of input ports or output ports of a device, are included around a programmable intellectual property (IP) core, only one MUX may be needed for each port near an input terminal of the programmable IP core. Therefore, the scan test circuit may be simplified to allow chip downsizing.

Specification, p. 14, lines 16-20. The independent claims have been amended above to more clearly recite the lack of synchronizing by the multiplexer coupling of an output of the core back to an input of the core.

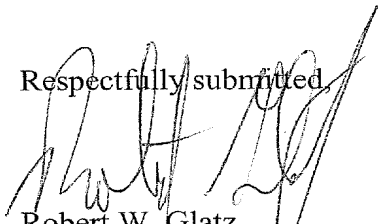
In contrast, the Pressly reference, while particularly directed to speed path test

circuitry, is analogous to the prior art described in the present application. In particular, Pressly proposes use of a wrapper circuit, where speed path test cells 16, 18 (or the alternative cell 32 of Figure 2 of Pressly) are provided for each input/output of the core 14. Pressly, Col. 6, lines 43-49; Col. 8, lines 14-27. Each of the cells 16, 18, 32 include synchronizing flip-flops 20, 22, 26, 28, 34, 36 in addition to the multiplexers, such as the multiplexer 42 of Figure 2 relied on in the rejections. Accordingly, the rejections of the independent claims, as amended above, should be withdrawn at least as Pressly fails to disclose the use of a multiplexer between the core block and the input side sub logic circuit without synchronizing a signal passed by the multiplexer to the core block. The dependent claims are patentable at least based on the patentability of the claims from which they depend.

CONCLUSION

Applicants respectfully submit that the reference cited in the present rejections does not disclose or suggest the present invention as claimed. Accordingly, Applicants respectfully request reconsideration of the rejections by the Examiner and allowance of all the pending claims and passing this application to issue.

Respectfully submitted,



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